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EXAMINER
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MOORE, IAN N

ART UNIT	PAPER NUMBER
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2416

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/646,833	<b>Applicant(s)</b> TRAN ET AL.	
	<b>Examiner</b> IAN N. MOORE	<b>Art Unit</b> 2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2009.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/24/09 has been entered.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

**Regarding claims 1-16, the applicant argued that,** "...CrystalClear fails to disclose or suggest a method for communication audio using a 2-line serial multi-channel audio interconnect data bus including a first signal line and a second signal line...wherein the first signal line and the second signal line form the 2-line serial multi-channel audio interconnect data bus structured to communication audio..." in page 5-7.

**In response to applicant's argument, the examiner respectfully disagrees** with the argument above.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re*

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*Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the combined system of CS4205 and Voth clearly discloses the claimed invention.

CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising: communication audio using a 2-line serial multi-channel audio interconnect data bus (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, **communicating serial audio over multiple channels/lines interconnecting bus**) including only a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, **includes SD data line (OUT, or SDOUT)**) and a second signal line (see FIG. 7,14, **SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK)**; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9) wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line are configured to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK) are used to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9; *note that per FIG. on cover page, FIG. 7, 14, SDATA\_OUT signal line and SYNC signal line are sufficient/enough for communicating audio data; note that RESET # signal line is utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not required and thus it is not used for communication audio. SDATA\_OUT signal line and SYNC signal line are used for communication audio; see page 13 section 2.1; alternatively, per FIG. on cover page; per FIG. 7, 14, SDOUT signal line and LRCLK signal line are used for communicating audio data; note that SCLK is optional in CS4205, and thus it is clear that SCLK signal is not required*

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*and thus it is not used for communication audio. SDATA\_OUT signal line and LRCLK signal line are used for communication audio; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7) form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio (see FIG. on cover page; see FIG. 7, 14; forming/configured as the serial audio over multiple channels/lines interconnecting bus to communicate/transmit/received audio data).*

Voth teaches communication using a 2-line serial multi-channel interconnect data bus (FIG. 2, a 2-line host-pedant system using serial multi-lines/channel interconnect data bus system 200) including only a first signal line (FIG. 2, data<sub>1</sub> bus at GPIO<sub>1</sub>) and a second signal line (FIG. 2, clock<sub>1</sub> bus at GPIO<sub>2</sub>); abstract; see col. 6, line 1-50); wherein only the first signal line and the second signal line (FIG. 2, data<sub>1</sub> bus at GPIO<sub>1</sub> and clock<sub>1</sub> bus at GPIO<sub>2</sub>) form the 2-line serial multi-channel interconnect data bus structured to communicate (FIG. 2, form/configure 2-line host-pedant system using serial multi-lines/channel interconnect data bus; see col. 6, line 1-50).

In view of the above, it is clear that the combined CS4205 and Voth clearly disclose the broadly claimed invention.

**The previous responses to the argument on CS4205 are hereby incorporated.**

***Claim Rejections - 35 USC § 101***

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

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**Claim 1** recites, "a **method of communication audio**, comprising: communicating audio....transmitting audio information....transmitting a number of synchronization markers..."

**Claim 12** recites, "a **method of communication audio**, comprising: communicating audio....receiving audio information....receiving a number of synchronization markers..."

Claims 1 and 12 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to particular machine, or (2) transform underlying subject matter (such as an article or material) to a different state or thing. See page 10 of In Re Bilski 88 USPQ2d 1385.

The instant claims are neither positively tied to a particular machine that accomplishes the claimed method steps nor transform underlying subject matter, and therefore do not qualify as a statutory process.

For example, the method including steps of "communicating audio....transmitting audio information....transmitting a number of synchronization markers..." and "communicating audio....receiving audio information....receiving a number of synchronization markers..." It is broad enough that the claim could be completely performed mentally, verbally or without a machine nor is any transformation apparent. Thus, the method claim

1) do not tied to particular machine (such as a particular apparatus) by identifying the apparatus (e.g. encoder or decoder) that accomplishes the method steps

**OR**

2) do not transform underlying subject matter (such as an article or material) to a different state or thing.

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Thus, claims 1 and 12 are non-statutory.

Claims 3-11 and 13-16 are also rejected since they are depended upon the rejected claims set forth above.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-4, 6, 8-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 (CyrstalClear Audio Codec '97 product information document) in view of Voth (US006957284B2).

**Regarding Claim 1**, CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

communication audio using a 2-line serial multi-channel audio interconnect data bus (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, communicating serial audio over multiple channels/lines interconnecting bus) including only a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, includes SD data line (OUT, or SDOUT)) and a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

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transmitting audio information segments on the first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line (OUT, or SDOUT) transmits each audio frame segment/portion/frame), each segment (see FIG. 14, 17-20, each audio frame) including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1, 4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

transmitting a number of synchronization markers (see FIG. 14, transmitting SYNC pluses; see FIG. 17-20, transmitting LRCLK pulses) on the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being representative of a timing of one of the audio information segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line are configured to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK) are used to communicate audio



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PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9; *note that per FIG. on cover page, FIG. 7, 14, SDATA\_OUT signal line and SYNC signal line are sufficient/enough for communicating audio data; note that RESET # signal line is utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not required and thus it is not used for communication audio. SDATA\_OUT signal line and SYNC signal line are used for communication audio; see page 13 section 2.1; alternatively, per FIG. on cover page; per FIG. 7, 14, SDOUT signal line and LRCLK signal line are used for communicating audio data; note that SCLK is optional in CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for communication audio. SDATA\_OUT signal line and LRCLK signal line are used for communication audio; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7) form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio (see FIG. on cover page; see FIG. 7, 14; forming/configured as the serial audio over multiple channels/lines interconnecting bus to communicate/transmit/received audio data).*

Although CS4205 discloses using “a first signal line and a second signal line” as set forth above,

CS4205 does not explicitly disclose using “*only*” a first signal line and a second signal line.

However, Voth teaches communication using a 2-line serial multi-channel interconnect data bus (FIG. 2, a 2-line host-pendant system using serial multi-lines/channel interconnect data

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bus system 200) including only a first signal line (FIG. 2, data<sub>1</sub> bus at GPIO<sub>1</sub>) and a second signal line (FIG. 2, clock<sub>1</sub> bus at GPIO<sub>2</sub>); abstract; see col. 6, line 1-50); .

wherien only the first signal line and the second signal line (FIG. 2, data<sub>1</sub> bus at GPIO<sub>1</sub> and clock<sub>1</sub> bus at GPIO<sub>2</sub>) form the 2-line serial multi-channel interconnect data bus structured to communicate (FIG. 2, form/configure 2-line host-pedant system using serial multi-lines/channel interconnect data bus; see col. 6, line 1-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide using “only” as taught by Voth in the system of CS4205, so that it would provide a general purpose, functional bus for chaining low-speed portable peripheral components; see Voth col. 1, line 40-60.

**Regarding Claim 2**, CS4205 Reference discloses the audio comprises a serial bit stream (see page 13, paragraph 2.1; audio stream is a serial bit stream).

**Regarding Claim 3**, CS4205 Reference discloses the information segments are unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5, 4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated in CS4205).

**Regarding Claim 4**, CS4205 Reference discloses the information segments are representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more audio channels/slots).

**Regarding Claim 6**, CS4205 Reference discloses wherein the format modes include at least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1,

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4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode)).

**Regarding Claim 8**, CS4205 Reference discloses the format modes are dynamic (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame, thus the audio format/arrangement/layout are dynamic).

**Regarding Claim 9**, CS4205 Reference discloses the format modes are configured to vary from one information segment to another information segment (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame).

**Regarding Claim 10**, CS4205 Reference discloses the synchronization marker include sync pulses (see FIG. 14, 17-20; each SYNC/LRCLK pulse; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

**Regarding Claim 11**, CS4205 Reference discloses each sync pulse represents a start of one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

**Regarding Claim 12**, CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

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communication audio using a 2-line serial multi-channel audio interconnect data bus (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, communicating serial audio over multiple channels/lines interconnecting bus) including only a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, includes SD data line (IN&OUT, or SDOOUT & SDI1-3)) and a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

receiving audio information segments on the first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line (IN&OUT, or SDOOUT & SDI1-3), each segment including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

receiving a number of synchronization markers (see FIG. 14, receiving SYNC pluses; see FIG. 17-20, transmitting LRCLK pulses) on the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being

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represented of a timing of one of the audio segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein only the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9) are used to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT\_CLK; or SCLK & LRCLK) are arranged/configured to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9); *note that per FIG. on cover page, FIG. 7, 14, SDATA\_OUT signal line and SYNC signal line are sufficient/enough for communicating audio data; note that RESET # signal line is utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not required and thus it is not used for communication audio. SDATA\_OUT signal line and SYNC signal line are used for communication audio; see page 13 section 2.1; Alternatively, per FIG. on cover page; per FIG. 7, 14, SDOUT signal line and LRCLK signal line are used for communicating audio data; note that SCLK is optional in CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for communication audio. Only SDATA\_OUT signal line and LRCLK signal line are used for communication audio; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7) form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio (see FIG. on cover page;*

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see FIG. 7, 14; forming/configured as the serial audio over multiple channels/lines interconnecting bus to communicate/transmit/received audio data).

Although CS4205 discloses using “a first signal line and a second signal line” as set forth above,

CS4205 does not explicitly disclose using “*only*” a first signal line and a second signal line.

However, Voth teaches communication using a 2-line serial multi-channel interconnect data bus (FIG. 2, a 2-line host-pedant system using serial multi-lines/channel interconnect data bus system 200) including only a first signal line (FIG. 2, data<sub>1</sub> bus at GPIO<sub>1</sub>) and a second signal line (FIG. 2, clock<sub>1</sub> bus at GPIO<sub>2</sub>); abstract; see col. 6, line 1-50); .

wherien only the first signal line and the second signal line (FIG. 2, data<sub>1</sub> bus at GPIO<sub>1</sub> and clock<sub>1</sub> bus at GPIO<sub>2</sub>) form the 2-line serial multi-channel interconnect data bus structured to communicate (FIG. 2, form/configure 2-line host-pedant system using serial multi-lines/channel interconnect data bus; see col. 6, line 1-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide using “only” as taught by Voth in the system of CS4205, so that it would provide a general purpose, functional bus for chaining low-speed portable peripheral components; see Voth col. 1, line 40-60.

**Regarding Claim 13**, CS4205 Reference discloses the information segments are unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5, 4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated in CS4205).

**Regarding Claim 14**, CS4205 Reference discloses the information segments are representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more audio channels/slots).

**Regarding Claim 16**, CS4205 Reference discloses each sync pulse represents a start of one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

7. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 in view of Voth and further in view of Wolf (US007088398B1).

**Regarding Claim 5**, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

Neither CS4205 nor Voth explicitly disclose “32 bits”.

However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the combined

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system of CS4205 and Voth, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

**Regarding Claim 15**, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

Neither CS4205 nor Voth explicitly disclose 32 bits.

However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the combined system of CS4205 and Voth, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 in view of Voth and further in view of Wakazu (US006006287A).

**Regarding Claim 7**, CS4205 Reference discloses wherein the format modes include at least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode)), and



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transmission of one or more one or more of the transmitted audio segments/frames to an intended recipient (see FIG. 7, controller, see FIG. 16, Stereo DACs) as set forth above in claim 1.

Neither CS4205 nor Voth explicitly disclose audio stream ID includes an indication of an intended recipient.

However, Wakazu teaches the audio stream ID (see FIG. 4, Audio stream ID 2; see FIG. 6, Audio stream IDs A1-A5) includes an indication of an intended recipient of one or more of the transmitted audio segments (see FIG. 2, audio stream ID indicates/identifies the receiver processor 211 or processor 210; see col. 5, line 10 to col. 6, line 60).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide audio stream ID includes an indication of an intended recipient, as taught by Wakazu in the combined system of CS4205 and Voth, so that it can separate/detect the received data stream according to the stream ID; see Wakazu col. 2, line 10-15, 40-49.

### ***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085.

The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick W. Ferris can be reached on 571-272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Ian N. Moore  
Primary Examiner  
Art Unit 2416

***/Ian N. Moore/  
Primary Examiner, Art Unit 2416***